CH₃NH₃PbI₃-based Perovskite Material Patterning and Thin-Film Transistor Fabrication

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ABSTRACT

We patterned a perovskite film to fabricate thin-film transistors (TFTs) and investigated the effect of patterning on the electrical performance of the TFTs. We used a simple and effective patterning method, i.e., wet-assisted mechanical exfoliation. The perovskite films with 3 different thicknesses were fabricated using spin coating at 1,000, 2,000, and 4,000 rpm. Finally, we evaluated the performance of these TFTs. It was estimated that the film fabricated at 1,000 rpm spinning speed had the highest performance. In the best case the mobility of the TFTs reached up to 2.11 cm²/V·s, and very much depends on the active channel size. The proposed patterning technique enables perovskite semiconductor materials to be used in high-density arrays. In addition, it can be used for the production of electronic devices in various fields.

Keywords: Perovskite patterning, Mechanical exfoliation, Thin-film transistor, Device performance

1. Introduction

Discovery of the active-matrix displays have led to the era of high-end displays and revolutionized the display industry. In this technology thin-film transistors (TFT) are used which play a key role and must fulfil several unique requirements [1,2]. The TFT is a field effect transistor and its structure and operation principles are similar to the metal oxide field effect transistor. The concept of the metal-insulator-semiconductor (active layer) field effect transistor was manifested in 1925 [3]. The early popular TFT versions were made of compound semiconductors such as CdS or CdSe [4]. However, this kind of display devices never went to mass production mainly caused by device reliability over large areas.

The breakthrough in this field was a report in 1979 where the first working TFT based on hydrogenated amorphous silicon (a-Si:H) was illustrated [5]. The composing films were deposited by plasma-enhanced chemical vapor deposition. Since then, the a-Si:H was widely used for manufacturing display devices [6]. The a-Si:H TFT has a field effect mobility (μ_{fe}) < 0.8 cm²/V·s, an off current (I_{off}) of < 10⁻¹² A, an on/off current ratio (I_{on}/I_{off}) of > 10⁶, a threshold voltage (V_{th}) of < 3 V, and a subthreshold slope (S) of < 0.5 V/dec [7,8]. These characteristics of the active layer is fully met with requirements for liquid-crystal display type of displays but not enough for organic light-emitting diode displays. To overcome the mobility, issue a technology called low-temperature polysilicon (LTPS) was developed [9,10]. This technology allows to fabricate polysilicon with mobility up to 50–400 cm²/V·s (more common 105 cm²/V·s); however, this technology involves several steps including laser crystallization (excimer laser) which makes this technology very expensive.

Furthermore, in the new generation of display devices where the display is flexible and has to be flexed the mechanical stability of the TFT becomes one of the critical parameters [11,12].

An alternative to silicon TFT, recently an amorphous metal-oxide-based [13–16] and organic semiconductor based TFT [17] have been extensively developing. For organic TFT (OTFT) the main pain point remains the low mobility and reliability and need further improvement [18–20].

One of the new class materials which can be a game-changer for TFT fabrication is organic-inorganic hybrid material such as perovskite material. The perovskite is most attractive due to its unique material properties such as a direct bandgap, large absorption coefficient, long exciton diffusion length, and carrier lifetime. Moreover, the processing is cost-effective, which is big advantages for mass production. The general chemical formula of perovskite can be represented as ABX₃, which forms a 3D network where A site ion inhabits the space between four adjacent corner-sharing BX₆ octahedra [21]. The A is typically a small organic cation methylammonium (MA or CH₃NH₃I⁺) or formamidinium [FA⁺ or (NH₂)₂CH⁺], B a large metal cation such

Figure 1. Bottom gate TFT structure utilizing (a) integral perovskite film and (b) patterned perovskite film. In order to observe the current characteristics according to the voltage, the positions of the gate, source, and drain of the transistor are indicated.

Figure 2. I_d - V_g curves of the transistors with perovskite active layer. The active layer was fabricated at (a) 1,000, (b) 2,000, and (c) 4,000 rpm by spin coating technique.

as Pb^{2+} or Sn^{2+} and X a halide anion (I^- , Br^- or Cl^-). The inorganic component forms strong covalent/ionic bonds while the organic component enables the self-assembly of these materials. As a result, it is possible to fabricate this film very simple, cost-effective way at low-temperature [22]. The charge transport parameters, i.e., carrier diffusion length for $MAPbI_3$ single crystals was estimated to be up to 175 μm and carrier lifetime was 2 μs [23, 24]. For the $MAPbI_3$ polycrystalline film, the diffusion length is estimated to be 1.2 μm and a carrier lifetime of 1 μs [25, 26] has been reported. The mobility for the single crystals $MAPbI_3$ and the $MAPbI_3$ polycrystalline films were estimated to be 24-800 $cm^2/V\cdot s$ and 1-71 $cm^2/V\cdot s$, respectively.

In the Wehrenfennig *et al.* [24] it is reported that a one-step spin-coated perovskite $CH_3NH_3PbI_3$ possesses 10^{-5} $cm^2/V\cdot s$ hole mobility. Extensive research has been done to improve the performance of perovskite TFTs [27, 28].

As texted above, in the active-matrix displays the TFTs play key role. Thus, each pixel is individually controlled by one to seven transistors. The TFT active-matrix array is made of millions of individual units. Individual elements are connected by gate lines along rows which operate the TFT, by drain lines along columns. The size, resolution and information content of the displays are strongly depending on the size of those TFTs and lines. Higher resolutions require smaller individual units. In this end, an effective method of patterning of all layers including active layer must be implemented. However, up to now patterning of the perovskite film is missing and need further development

In this work, we suggested and implemented a new method for patterning the perovskite film. For the fabrication of the perovskite film, we used our methods reported in [29, 30]. Patterned perovskite films were successfully used to manufacture the TFT.

2. Experiments

A heavily boron-doped p-type semiconductor wafer ($< 0.005 \Omega\cdot cm$) was used as a substrate. Surface contamination was removed by employing reactive ion etching using oxygen plasma. The plasma treatment was performed at room temperature under a vacuum of 10^{-3} Torr. The power and duration of the treatment were 250 W and 90 s, respectively. After clearing, a 1,000 Å thin oxide film was formed via dry oxidation. A $CH_3NH_3PbI_3$ film was deposited on the substrate when the substrate was ready. CH_3NH_3I and PbI_2 (1:1 weight ratio) in dimethyl sulfoxide (DMSO) and γ -butyrolactone (3:7 M ratio) mixed solvents were mixed. Then, the substrate was spin coated with the solution at speeds of 1,000, 2,000, and 4,000 rpm for 60 s. The film was formed after 25 s. Next, toluene was dropped on the formed film to eliminate the residue solvent and DMSO. Thereafter, the film was annealed at 100°C for 120 min to complete the formation of the semiconductor material. The film thickness was determined using transmission electron microscopy (TEM), and it was estimated to be approximately 200 nm for a spin speed of 4,000 rpm [30].

The perovskite films were divided in two groups. One group was non-patterned, and the other group was patterned to form an active layer. On both groups of perovskite films, 100 nm Ag thin films were deposited as source and drain materials using metal masks and electron beam deposition. A metal mask was placed on the perovskite film at the location where Ag would be deposited. The base pressure before deposition and the operating pressure during deposition were $\sim 10^{-6}$ and $\sim 10^{-3}$ Torr, respectively. The process temperature was 25°C, and the substrate rotation speed was adjusted to be 5 rpm to form a uniform film. This set of parameters provided a deposition rate of 1 Å/s.

As mentioned earlier, one of the main purposes of this study was the fabrication of patterned perovskite TFTs. As shown in Fig. 1, a bottom-gate TFT was fabricated by utilizing an unetched semiconductor material [Fig. 1(a)] and patterned active layers [Fig. 1(b)].

3. Results and discussion

We examined the electrical performance of the bottom-gate TFT. In particular, we measured the electrical performance of nonpatterned and patterned active layers to understand the suitability of mechanical exfoliation for patterning. In addition, we examined the effect of the thickness of the active layer.

3.1. I_d - V_g curves of TFTs fabricated using nonpatterned perovskite films

Figure 2 shows the drain current (I_d)-gate voltage (V_g) curves of the TFTs fabricated using nonpatterned perovskite films. The red and black curves were obtained at a drain voltage (V_d) of -1.0 and -0.1 V, respectively. Figures 2(a)-(c) show the results obtain at spin speeds of 1,000, 2,000, and 4,000 rpm. The best TFT performance in terms of the on and off characteristics was obtained for the films fabricated at 1,000 rpm. Therefore, this speed was selected to fabricate the semiconductor layer for further investigation. An extremely similar TFT performance

Figure 3. Top-view SEM results for (a) low and (b) high magnifications of the mechanically exfoliated perovskite pattern. Perovskite thin films were coated at 1,000 rpm process conditions. (b) is an image of a detailed observation of the etching area shown in (a), and the numbers 1, 2, and 3 are indicated for EDS analysis in Fig. 4.

Figure 4. EDX spectra of patterned perovskite (a) the perovskite film, (b) the edge of the perovskite film, and (c) the liberated substrate.

was reported in a previous study [31], where the effect of the pressure on annealing was discussed.

3.2. I_d - V_g curves of TFTs fabricated using patterned perovskite films

Wet-assisted mechanical exfoliation was used to pattern the perovskite film. The pattern quality was examined using a scanning electron microscope (SEM) linked with an energy-dispersive X-ray (EDX) analysis gun. Figure 3 shows the SEM images of the patterned perovskite film. The perovskite film was successfully patterned using wet-assisted mechanical exfoliation. A brush was soaked in isopropyl alcohol solution then applied to pattern the film. EDX analysis was performed at 3 points [Fig. 3(b)] to confirm that the perovskite was fully removed, i.e., (1) the film, (2) edge of the film, and (3) liberated substrate. Figure 4 illustrates the EDX spectra at these 3 points. After patterning, the perovskite film was completely removed, and a well-formed semiconductor pattern was obtained [Fig. 4(c)]. The component results of the EDX analyses are summarized in Table I.

As shown in Fig. 5, the length and width of the fabricated TFT were 850 and 1,410 μm , respectively. Figure 6 shows the transfer and output curves of this TFT. These curves were similar to those of an enhanced mode p-channel transistor. They were composed of linear

Figure 5. Optical microscopy image and dimension of the TFT.

Figure 6. (a) Transfer and (b) output curves for patterned perovskite-based TFTs.

and saturated regions except for a small change. We analyzed changes in I_d with V_g to derive the physical parameters for TFTs. The measured device parameters are summarized in Table II. The V_{th} was defined as the value of V_g at which $I_d = 10$ nA at $V_d = -1$ V. The μ_{fe} of these TFTs was estimated from Eq. (1) [32].

$$\mu_{fe} = L_c t_c / (W_c C_{go} V_d) \quad (1)$$

Here, t_c is the transconductance. W_c and L_c are the channel width and length, respectively. C_{go} is the gate oxide capacitance per unit area. The S factor, which is the defect state at the interface between the gate oxide and perovskite material, is generally sensitive to the density of defects at the interface. Subthreshold slope S is expressed as

$$S = kT/q \cdot \ln 10 (1 + q^2 N_t / C_{go}), \quad (2)$$

where q is the electronic charge value, k is the Boltzmann constant, T is the absolute temperature, and N_t is the density of trap states per unit area and per eV [33]. The calculated defect density was estimated to be $\sim 10^{-13} \text{ eV}^{-1} \cdot \text{cm}^{-2}$. The active channel material had a high density of gap states, and the oxide formed a poor interface with the perovskite film. This implies that perovskite films and optimal gate insulating films must be developed. The I_{off} was assumed to be the lowest current value.

Table I. Elements concentration in the patterned film; point (1) the perovskite film, point (2) the edge of the perovskite film, and point (3) the liberated substrate.

Wt. %	C-K	N-K	O-K	Na-K	Si-K	Pd-L	I-L	W-M	Pb-M
point (1)	0.27	0.00				2.99	43.30	31.05	22.38
point (2)	2.51	0.00					59.83		37.66
point (3)			13.62	0.08	86.30				
At %	C-K	N-K	O-K	Na-K	Si-K	Pd-L	I-L	W-M	Pb-M
point (1)	3.39	0.00				4.20	51.01	25.25	16.15
point (2)	24.22	0.00					54.70		21.08
point (3)			21.67	0.09	78.24				

Table II. Device parameters of patterned perovskite-based TFTs for $W_c/L_c = 1,410 \mu\text{m}/850 \mu\text{m}$.

TFT parameter			
V_{th} (V)	μ_{fe} (cm^2/Vs)	S factor (V/dec)	I_{on}/I_{off}
-3.5	0.23	1.3	2.2×10^6

Table III. Device parameters of patterned perovskite based TFTs for $W_c/L_c = 1,530 \mu\text{m}/690 \mu\text{m}$.

TFT parameter			
V_{th} (V)	μ_{fe} (cm^2/Vs)	S factor (V/dec)	I_{on}/I_{off}
-2.7	2.11	0.96	5.7×10^6

I_d was expressed using the relationship between V_d and V_g in the linear region. The output curve equation is given by [32].

$$I_d = W_c/L_c \cdot C_{go} \mu_{cm} (V_g - V_{tv} - V_d/2) V_d. \quad (3)$$

As I_d is proportional to W_c/L_c , the current characteristics can be improved by changing the size of the TFT. The kink effect appeared when V_g was -20 V and V_d was -10 V.

Figure 7 shows another structure of the TFT. The device parameters are summarized in Table III. The channel width was increased by approximately 8.5%, and the length was decreased by approximately 23%. The I_{on}/I_{off} ratio was improved by approximately 2.5 times by increasing I_{on} , where I_d was proportional to W_c/L_c as given by Eq. (3). The charge mobility of this TFT was estimated to be $2.11 \text{ cm}^2/\text{V}\cdot\text{s}$ [Fig. 8(b)]. All characteristics were improved when the length of the TFT was increased instead of the width.

4. Conclusion

We developed a method for patterning a hybrid metal-halide perovskite ($\text{CH}_3\text{NH}_3\text{PbI}_3$) film. The film was fabricated via spin coating. The thickness of the film was controlled by adjusting the spin speed. The film fabricated at a spin speed of 1,000 rpm showed the best electrical properties; hence, this speed was used for further investigation. Wet-assisted mechanical exfoliation was optimized and implemented to pattern the film.

Using the patterned semiconductor material, TFTs with two different dimensions were created, and their electrical performances were measured. The charge mobility of the TFTs improved from 0.23 to $2.11 \text{ cm}^2/\text{V}\cdot\text{s}$ when the channel dimensions were changed. The results of

Figure 7. Optical microscopy image and dimension of the TFT. **Figure 8.** (a) Transfer curve and (b) charge mobility of patterned TFTs.

this study can provide a new direction for improving the performance of devices based on perovskites.

To further improve the properties of the TFTs, it is necessary to develop a gate insulation layer that forms a suitable interface for perovskite semiconductors. In addition, etching techniques must be examined to produce small-size elements for applications in various fields.

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Conflicts of Interest

The authors declare no conflicts of interest.

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